

Specification

The purpose of this purchase request is to acquire the components of a data acquisition and signal generation system. The overall configuration of the system can be divided into three subsystems: ADC, DAC and PPC. The general descriptions of these subsystems are: 1. a number of analog-to-digital converters (ADCs) with an associated Field Programmable Gate Array (FPGA), 2. a number of digital-to-analog converters (DACs) with an associated FPGA and 3. a PowerPC (PPC) with an associated FPGA. Each of the three independent FPGAs shall be connected together through various I/O configurations. The specifications and requirements for each of these subsystems are as follows:

1. ADC Subsystem

- a. The ADC Subsystem shall contain a Virtex-6 FPGA, XC6VLX240T or better. The FPGA must be connected at a minimum by 21 differential LVDS pairs to the PPC and DAC subsystem FPGAs. Both flash memory and a JTAG connector must be provided to program the FPGA. The FPGA must also be connected to any other FPGA and to the PPC by PCI Express (PCIe) (4-lane).
- b. The subsystem shall contain at least 10 ADCs, each providing 16 bits at a rate of at least 160 million samples per second (MSPS). These ADCs shall interface directly with one of the provided FPGAs that are not directly connected to the DACs or PPC. SMA connectors with 50 ohm input impedance shall provide inputs to the ADCs.
- c. The subsystem shall provide at least 2 programmable SMA input triggers, at least 2 programmable SMA output triggers and a programmable DB25 connected directly to the FPGA.
- d. There shall be a minimum of 512 MB of DDRII memory connected directly to the FPGA.
- e. The ADC subsystem must provide the ability to increase the number of ADCs in increments of 10.

2. DAC Subsystem

- a. The DAC Subsystem shall contain at a Virtex-6 FPGA, XC6VLX240T or better. The FPGA must be connected at a minimum by 21 differential LVDS pairs to the PPC and ADC subsystem FPGAs. Both flash memory and a JTAG connector must be provided to program the FPGA. The FPGA must also be connected to any other FPGA and to the PPC by PCIe (4-lane).
- b. The system shall contain at least 2 DACs, each accepting 16-bit input data at a rate of at least 250 MSPS. These DACs shall interface directly with one of the provided FPGAs that are not directly connected to the ADCs or PPC. Each DAC shall be able to drive a 50 ohm load and provide its output on an SMA connector.
- c. The FPGA directly connected to the DACs shall have a minimum of 10 programmable SMA connections for user I/O. Also two independent, programmable purpose I/O connectors shall be provided to this FPGA.

3. PPC Subsystem

- a. The PPC Subsystem shall contain at a Virtex-6 Field Programmable Gate Arrays (FPGA), XC6VLX240T or better. The FPGA must be connected at a minimum by 21 differential LVDS pairs to the DAC and ADC subsystem FPGAs. Both flash memory and a JTAG connector must be provided to program the FPGA. The FPGA must also be connected to any other FPGA and to the PPC by PCIe (by-4).
- b. The system shall contain at least 1 PowerPC processor for system control. The processor shall be provided with at least two 1 gigabit-per-second Ethernet (1GigE) communication channels and at least one RS-232 communication channel. The PPC shall interface directly with all three FPGAs through PCIe (4-lane).
- c. The PPC shall have a minimum of 2GB of DDR memory.
- d. The FPGA associated with the PPC shall have a minimum 2 programmable SMA input connections and 2 programmable SMA output connections.
- e. There shall be a minimum of 512MB DDRII memory connected directly to the FPGA that is not shared with the PPC.

4. The system shall provide board level monitoring of temperature and voltage and provide self-protection for over temperature and over voltage.
5. VHDL source code for all FPGA drivers and PPC Linux drivers must be provided.